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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,903	02/27/2002	Carl Mizuyabu	1376.0200100	4958

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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,903	MIZUYABU ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) *24-35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22,36-49 and 51-54* is/are rejected.

7)☒ Claim(s) *50* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in responsive to request for continuing examination [RCE] filed on 11 July 2005.

2. Claims 24 – 35 have been cancelled.

3. Claims 1 – 23, and 36 – 54 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 8,13 – 14, 19 – 20, and 36 – 37, are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Challen, US Patent 4,521,918.

5. As to claim 1, Challen discloses a method comprising:

a. determining [based on conditions] a power mode for a device [col. 5, lines 34 – 43];

b. disabling a phase looked loop by reducing [removing] power used for driving the phase locked loop and providing an oscillator signal to drive a clock line when in a first power mode [battery save operation][col. 4, lines 62 – 67]; and

c. providing the oscillator signal to an input of the phase locked loop [during battery save operation] and providing a locked signal from an output of the phase locked loop to the clock line when in a second power mode [normal operations][col. 3, lines 11 – 51, col. 4, lines 19 – 21, 34 – 67, col. 5, lines 1 – 48, fig. 2].

6. As to claim 36, Challen discloses a device and method computer readable medium tangibly embodying a program instructions to manipulate a system to:

a. determining [based on conditions] a power mode for a device [col. 5, lines 34 – 43];

b. disabling a phase looked loop by shutting [removing] power used for driving the phase locked loop and providing an oscillator signal to drive a clock line when in a first power mode [battery save operation][col. 4, lines 62 – 67]; and

c. providing the oscillator signal to an input of the phase locked loop [during battery save operation] and providing a locked signal from an output of the phase locked loop to the clock line when in a second power mode [normal operations][col. 3, lines 11 – 51, col. 4, lines 19 – 21, 34 – 67, col. 5, lines 1 – 48, fig. 2].

7. As to claims 2, and 37, Challen discloses that the device consumes less power in the first power mode [power save operation] than in the second power mode [normal operations][col.5, lines 8 – 10].

8. As to claim 3, Challen's mobile phone inherently teaches the suspending processing within the device when in a third power mode during the power off condition.

9. As to claims 4 – 5, Challen discloses to generate oscillator signal using local oscillator including crystal oscillator, an RC circuit [col. 1, lines 9 – 16].

10. As to claims 6 – 7, Challen discloses a phased-locked loop [10, PLL] including a phase comparator, and dividers and multiplexers [col. 1, lines 45 – 48], therefore he teaches the arrangement and connection of different components and signals too.

11. As to claim 8, Challen discloses disabling the phased lock loop [PLL], when in the first power mode [battery save operation] including providing reduced [interrupt] power, in comparison to an available power [full power for normal operation][col. 3, lines 11 – 24].

12. As to claim 13, Challen discloses the device used in a portable device such as mobile telephone [col. 3, lines 11 – 12].

13. As to claim 14, Challen discloses the device used in a portable device such as mobile telephone [col. 3, lines 11 – 12] therefore he teaches a personal digital assistant too.

14. As to claim 19, Challen discloses disabling the phased locked loop [PLL] including shutting off power [with switch open] used for driving the PLL [col. 4, lines 62 – 67, col. 5, lines 1 – 11, fig. 2].

15. As to claim 20, Challen discloses to provide an oscillator signal to drive clock line [output] includes coupling a line carrying the oscillator signal [VCO out] to the clock line [output] [fig. 2].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

16. Claims 44 – 45, 47 – 48, and 52 – 54, are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,215 B1 [cited in previous office action], and further in view of Challen, US Patent 4,521,918.

17. As to claim 44 Mirov discloses a system comprising: (a) a phase locked loop [PLL] having a first input to receive a first clock signal [CLOCK IN] and a first output to provide a second clock signal [CLOCK OUT], wherein the second clock signal [CLOCK OUT] is based on the first clock signal [CLOCK IN]; (b) a first multiplexer [1010] having a first input coupled to thee first input [CLOCK IN] of the phase locked loop [PLL], a second input coupled to the first output of the phase locked loop [CLOCK OUT] and an output, wherein the first multiplexer [1010] is operable to selectively provide [by asserting/deasserting PLL BYPASS signal to selectively output one of the two inputs] lo the output a signal received at the first input when in a first power mode [idle mode] or a signal received at the second input [second input of 1010 which is output from 1008] when in a second power mode [active mode]; and means [by asserting PLL BYPASS signal] for disabling the phase locked loop when in the first power mode [idle mode][col. 4, lmines 43 - 67, col. 5, lines 1 - 8, col. 6, lines 49 - 67, col. 7, lines 1 - 20, col. 8, lines

65 - 67, col . 9, lines 1 - 14, col. 13, lines 14 - 52, col. 15, lines 64- 67, col. 16, lines 1 - 67, co! . 17, lines 1 - 54, fig. 5, 10].

However, Mirov does not teach explicitly disabling of PLL by reducing power used for driving the PLL when in first power mode.

Challen teaches battery saving in frequency synthesizer including a disabling PLL by removing power during battery save operation [first power mode][col. 3, lines 11 – 51, col. 4, lines 19 – 21, 34 – 67, col. 5, lines 1 – 48, fig. 2].

It would have been obvious to one of ordinary skill in art, having the teachings of Mirov and Challen before him at the time of invention was made, to modify the disabling of PLL disclosed by Mirov to include removing power during battery save operation [first power mode] as taught by Challen, in order to obtain frequency synthesizer without substantial drift and can be relocked in short period of time [abstract, col. 1, lines 53 – 67, col. 2, lines 1 - 15].

18. As to claim 45, Mirov discloses a first clock divider [1006] and coupling of an output of first multiplexer [1010][co1. 12, lines 54 - 57, fig. 5].

19. As to claim 47, Mirov discloses a means [register bits] for determining a power mode [normal, reduced power mode, idle mode, reserved mode, as shown in table 1] of the system and means [asserting/deasserting PLL BYPASS signal] for providing a control signal [PLL BYPASS] to the first multiplexer based on the determined power mode [col. 6, lines 49 - 67, col. 17, lines 26 – 41].

20. As to claim 48, Mirov teaches means for determining a power mode of the system including means [software] for determining a number of pending instructions

[maximum utilization and underutilization][col. 4, lines 4, lines 31 - 50, col. 6, lines 49 - 67, col. 7, lines 1 - 24, col. 17, lines 26 – 41]

21. As to claim 52, Challen discloses disabling the phased lock loop including a means [60, switch] for shutting off a supply of power to PLL [fig. 2].

22. As to claim 53, Mirov discloses an oscillator [506] having and output coupled to the input of the phased lock loop [PLL], and is operable to output the first clock signal [col. 9, lines 15 - 35, fig. 5].

23. As to claim 54, Challen discloses a means [40, 60, switch] for disabling an output of the first clock signal [VCO output] by the oscillator [12, VCO] when in first power [battery save] mode [fig. 2].

24. Claims 46, is rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,215 B1 [cited in previous office action], and Challen, US Patent 4,521,918 as applied to claim 44 and further in view of Zhang et al. [hereinafter as Zhang], US Patent 6,687,322 [cited in previous office action].

25. As to claim 44 Mirov discloses a system comprising: (a) a phase locked loop [PLL] having a first input to receive a first clock signal [CLOCK IN] and a first output to provide a second clock signal [CLOCK OUT], wherein the second clock signal [CLOCK OUT] is based on the first clock signal [CLOCK IN]; (b) a first multiplexer [1010] having a first input coupled to thee first input [CLOCK IN] of the phase locked loop [PLL], a second input coupled to the first output of the phase locked loop [CLOCK OUT] and an output, wherein the first multiplexer [1010] is operable to selectively provide [by asserting/deasserting PLL BYPASS signal to selectively output one of the two inputs] lo

the output a signal received at the first input when in a first power mode [idle mode] or a signal received at the second input [second input of 1010 which is output from 1008] when in a second power mode [active mode]; and means [by asserting PLL BYPASS signal] for disabling the phase locked loop when in the first power mode [idle mode][col. 4, lines 43 - 67, col. 5, lines 1 - 8, col. 6, lines 49 - 67, col. 7, lines 1 - 20, col. 8, lines 65 - 67, col . 9, lines 1 - 14, col. 13, lines 14 - 52, col. 15, lines 64- 67, col. 16, lines 1 - 67, co! . 17, lines 1 - 54, fig. 5, 10].

However, Mirov does not teach explicitly disabling of PLL by reducing power used for driving the PLL when in first power mode.

Challen teaches battery saving in frequency synthesizer including a disabling PLL by removing power during battery save operation [first power mode][col. 3, lines 11 – 51, col. 4, lines 19 – 21, 34 – 67, col. 5, lines 1 – 48, fig. 2].

However, neither Mirov nor Challen teaches a second multiplexor having a first input/output buffer coupled to the input/output buffer of the oscillator, a second input/putput buffer coupled to the second input output buffer of the phase locked loop and a third input/output buffer, said multiplexor to: when in a first power mode, pass said source clock signal to said third input/output buffer, and when in a second power mode, pass said locked clock signal to said third input/output buffer; a second clock line coupled to the third input/output buffer of the second multiplexor.

Zhang discloses dual mode clock alignment and distribution with a second multiplexor [510] having a first input/output buffer coupled to the input/output buffer [502] of the oscillator, a second input/output buffer coupled to the second input output

buffer of the phase locked loop [PLLOUT] and a third input/output buffer, said multiplexor to: when in a first power mode glow speed), pass said source clock signal to said third input/output buffer [514]; and when in a second power mode [high speed], pass said locked clock signal to said third input/output buffer; a second clock line [CLKO] coupled to the third input/output buffer [514] of the second multiplexor [510] [col. 5, lines 9 - 67, col. 6, lines 1 - 60, fig. 5].

It would have been obvious to one of ordinary skill in art, having the teachings of Mirov, Challen, and Zhang before him at the time of invention was made, to modify the PLL circuit arrangement for battery saving frequency synthesizer to include a second multiplexor as taught by Zhang in order to obtain dual mode clock alignment and distribution devices bypasses the PLL and generates clock with sufficient margins to accommodate the requirements of the PCI mode and support both lower speed PCI clocking mode and the higher speed PCI-X clocking mode to provide substantial savings in cost while reducing circuit complexity [co. 3, lines 34 – 51].

26. Claims 48 – 49, are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,215 B1 [cited in previous office action], and Challen, US Patent 4,521,918 as applied to claim 44 and further in view of Durham et al. (hereinafter as Durhamq, US Patent 6,785,829 B1 [cited in previous office action].

27. As to claims 48 – 49, Mirov discloses a system comprising: (a) a phase locked loop [PLL] having a first input to receive a first clock signal [CLOCK IN] and a first output to provide a second clock signal [CLOCK OUT], wherein the second clock signal

[CLOCK OUT] is based on the first clock signal [CLOCK IN]; (b) a first multiplexer [1010] having a first input coupled to thee first input [CLOCK IN] of the phase locked loop [PLL], a second input coupled to the first output of the phase locked loop [CLOCK OUT] and an output, wherein the first multiplexer [1010] is operable to selectively provide [by asserting/deasserting PLL BYPASS signal to selectively output one of the two inputs] lo the output a signal received at the first input when in a first power mode [idle mode] or a signal received at the second input [second input of 1010 which is output from 1008] when in a second power mode [active mode]; and means [by asserting PLL BYPASS signal] for disabling the phase locked loop when in the first power mode [idle mode][col. 4, lines 43 - 67, col. 5, lines 1 - 8, col. 6, lines 49 - 67, col. 7, lines 1 - 20, col. 8, lines 65 - 67, col . 9, lines 1 - 14, col. 13, lines 14 - 52, col. 15, lines 64- 67, col. 16, lines 1 - 67, co! . 17, lines 1 - 54, fig. 5, 10].

However, Mirov does not teach explicitly disabling of PLL by reducing power used for driving the PLL when in first power mode.

Challen teaches battery saving in frequency synthesizer including a disabling PLL by removing power during battery save operation [first power mode][col. 3, lines 11 – 51, col. 4, lines 19 – 21, 34 – 67, col. 5, lines 1 – 48, fig. 2].

However, neither Mirov nor Challen teaches explicitly identifying a number of pending instructions, and type of instructions as the power mode [battery save] determining condition.

Durham teaches method and apparatus with low power mode identifying circuit [determining low power mode] including power audit and control circuit for monitoring

power dissipation of functional unit within processor. The low power mode circuit [234] examines the low power mode enable signal, the request signal and determiine the best time to enter the low power mode depending upon types and number of pending operations or instructions to be performed by the functional unit [col. 6, lines 41 - 67, col. 7, lines 1 - 16, col. 2, lines 4 - 35, col. 3, lines 26 - 67, col. 4, lines 1 – 24].

It would have been obvious to one of ordinary skill in art, having the teachings of Challen and Durham before him at the time of invention was made, to modify the device and method for reducing power consumption disclosed by Challen to include a power audit and control circuit for power monitoring including steps of determining types and number of pending instructions to be performed and determine the best time to enter the low power mode as taught by Durham in order to obtain self audit and control of power within functional unit of processor for selectively entering low power mode on per functional unit basis to reduce power dissipation of functional unit [col. 1 , lines 57 – 64] and each unit can implement its own power dissipation savings easier and more efficiently than central power dissipation control unit [col. 3, lines 44 – 62].

28. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,215 B1 [cited in previous office action], and Challen, US Patent 4,521,918 as applied to claim 44 and further in view of Anwyl et al. [hereinafter as Anwyl], US Patent 5,576,738[cited in previous office action].

29. As to claim 51, Mirov discloses a system comprising: (a) a phase locked loop [PLL] having a first input to receive a first clock signal [CLOCK IN] and a first output to provide a second clock signal [CLOCK OUT], wherein the second clock signal [CLOCK

OUT] is based on the first clock signal [CLOCK IN]; (b) a first multiplexer [1010] having a first input coupled to thee first input [CLOCK IN] of the phase locked loop [PLL], a second input coupled to the first output of the phase locked loop [CLOCK OUT] and an output, wherein the first multiplexer [1010] is operable to selectively provide [by asserting/deasserting PLL BYPASS signal to selectively output one of the two inputs] lo the output a signal received at the first input when in a first power mode [idle mode] or a signal received at the second input [second input of 1010 which is output from 1008] when in a second power mode [active mode]; and means [by asserting PLL BYPASS signal] for disabling the phase locked loop when in the first power mode [idle mode][col. 4, lines 43 - 67, col. 5, lines 1 - 8, col. 6, lines 49 - 67, col. 7, lines 1 - 20, col. 8, lines 65 - 67, col . 9, lines 1 - 14, col. 13, lines 14 - 52, col. 15, lines 64- 67, col. 16, lines 1 - 67, co! . 17, lines 1 - 54, fig. 5, 10].

However, Mirov does not teach explicitly disabling of PLL by reducing power used for driving the PLL when in first power mode.

Challen teaches battery saving in frequency synthesizer including a disabling PLL by removing power during battery save operation [first power mode][col. 3, lines 11 – 51, col. 4, lines 19 – 21, 34 – 67, col. 5, lines 1 – 48, fig. 2].

However, neither Mirov nor Challen teaches explicitly identifying a change in display content as the power mode [battery save] determining condition.

Anwyl teaches system with display apparatus with means for detecting changes in image content between successive frames of input video and method of determining the power mode of display device gby bringing out of low power Etstandby mode" in

response to change in screen content to displayed[col. 4, lines 44 - 67, col. 5, lines 1 – 16].

It would have been obvious to one of ordinary skill in art, having the teachings of Mirov, Challen and Amwyl before him at the time of invention was made, to modify to modify the device and method for reducing power consumption disclosed by Mirov and Challen to include activation/deactivation of low power mode based on identifying a change in display content [change in screen content between successive frame input video signals] as disclosed by Anwyl in order to obtain a display with power management for controlling display circuitry [col. 4, lines 44 - 67, col. 5, lines 1 – 16].

30. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Challen, US Patent 4,521,918 as applied to claim 1, as above.

31. As to claim 14, Challen discloses an apparatus and method for battery [power] saving of an cellular radio [electronic device] such as mobile telephone [portable] drawing power from battery [battery operated] [col. 3, lines 11 – 15] but does not explicitly include personal digital assistant [PDA]. The examiner takes Ofticial Notice that personal digital assistant device [PDA] is well-known types of battery operated portable device. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of invention to use personal digital assistant device for the cellular radio [electronic device] such as mobile telephone [portable] disclosed by Challen.

32. Claims 21, 22, 41, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Challen, US Patent 4,521,918 as applied to claims 1, 36, and 44

above, and further in view of Durham et al. (hereinafter as Durhamq, US Patent 6,785,829 B1 [cited in previous office action].

33. As to claims 21, 22, 41, and 43, Challen discloses a device and method of determining [based on conditions] a power mode for a device [col. 5, lines 34 – 43]; disabling a phase looked loop by reducing [removing] power used for driving the phase locked loop and providing an oscillator signal to drive a clock line when in a first power mode [battery save operation][col. 4, lines 62 – 67]; and providing the oscillator signal to an input of the phase locked loop [during battery save operation] and providing a locked signal from an output of the phase locked loop to the clock line when in a second power mode [normal operations][col. 3, lines 11 – 51, col. 4, lines 19 – 21, 34 – 67, col. 5, lines 1 – 48, fig. 2].

However, Challen does not teach explicitly identifying a number of pending instructions, and type of instructions as the power mode [battery save] determining condition.

Durham teaches method and apparatus with low power mode identifying circuit [determining low power mode] including power audit and control circuit for monitoring power dissipation of functional unit within processor. The low power mode circuit [234] examines the low power mode enable signal, the request signal and determine the best time to enter the low power mode depending upon types and number of pending operations or instructions to be performed by the functional unit [col. 6, lines 41 - 67, col. 7, lines 1 - 16, col. 2, lines 4 - 35, col. 3, lines 26 - 67, col. 4, lines 1 – 24].

It would have been obvious to one of ordinary skill in art, having the teachings of Challenge and Durham before him at the time of invention was made, to modify the device and method for reducing power consumption disclosed by Challenge to include a power audit and control circuit for power monitoring including steps of determining types and number of pending instructions to be performed and determine the best time to enter the low power mode as taught by Durham in order to obtain self audit and control of power within functional unit of processor for selectively entering low power mode on per functional unit basis to reduce power dissipation of functional unit [col. 1 , lines 57 – 64] and each unit can implement its own power dissipation savings easier and more efficiently than central power dissipation control unit [col. 3, lines 44 – 62].

34. Claims 23, and 42, are rejected under 35 U.S.C. 103(a) as being unpatentable over Challenge, US Patent 4,521,918 as applied to claims 1, and 36 above, and further in view of Amyl et al. [hereinafter as Amyl], US Patent 5,576,738 [cited in previous office action].

35. As to claims 23, and 42, Challenge discloses a device and method of determining [based on conditions] a power mode for a device [col. 5, lines 34 – 43]; disabling a phase looked loop by reducing [removing] power used for driving the phase locked loop and providing an oscillator signal to drive a clock line when in a first power mode [battery save operation][col. 4, lines 62 – 67]; and providing the oscillator signal to an input of the phase locked loop [during battery save operation] and providing a locked signal from an output of the phase locked loop to the clock line when in a second power

mode [normal operations][col. 3, lines 11 – 51, col. 4, lines 19 – 21, 34 – 67, col. 5, lines 1 – 48, fig. 2].

However, Challenge does not teach explicitly identifying a change in display content as the power mode [battery save] determining condition.

Amyl teaches system with display apparatus with means for detecting changes in image content between successive frames of input video and method of determining the power mode of display device by bringing out of low power "standby mode" in response to change in screen content to displayed][col. 4, lines 44 - 67, col. 5, lines 1 – 16].

It would have been obvious to one of ordinary skill in art, having the teachings of Challen before him at the time of invention was made, to modify to modify the device and method for reducing power consumption disclosed by Challen to include activation/deactivation of low power mode based on identifying a change in display content [change in screen content between successive frame input video signals] as disclosed by Anwyl in order to obtain a display with power management for controlling display circuitry [col. 4, lines 44 - 67, col. 5, lines 1 – 16].

36. Claims 9 – 12, 15 - 18, and 38 – 40, are rejected under 35 U.S.C. 103(a) as being unpatentable over Challen, US Patent 4,521,918 as applied to claims 1, and 36, above, and further in view of Zhang et al. [hereinafter as Zhang], US Patent 6,687,322 [cited in previous office action].

37. As to claims 9 – 12, 15 - 18, and 38 – 40, Challen discloses a device and method of determining [based on conditions] a power mode for a device [col. 5, lines 34 – 43]; disabling a phase looked loop by reducing [removing] power used for driving the phase

locked loop and providing an oscillator signal to drive a clock line when in a first power mode [battery save operation][col. 4, lines 62 – 67]; and providing the oscillator signal to an input of the phase locked loop [during battery save operation] and providing a locked signal from an output of the phase locked loop to the clock line when in a second power mode [normal operations][col. 3, lines 11 – 51, col. 4, lines 19 – 21, 34 – 67, col. 5, lines 1 – 48, fig. 2].

However, Challen does not teach explicitly to use a second multiplexor having a first input/output buffer coupled to the input/output buffer of the oscillator, a second input/output buffer coupled to the second input output buffer of the phase locked loop and a third input/output buffer, said multiplexor to: when in a first power mode, pass said source clock signal to said third input/output buffer', and when in a second power mode, pass said locked clock signal to said third input/output buffer; a second clock line coupled to the third input/output buffer of the second multiplexor.

Zhang discloses dual mode clock alignment and distribution with a second multiplexor [510] having a first input/output buffer coupled to the input/output buffer [502] of the oscillator, a second input/output buffer coupled to the second input output buffer of the phase locked loop [PLLOUT] and a third input/output buffer, said multiplexor to: when in a first power mode glow speed), pass said source clock signal to said third input/output buffer [514]; and when in a second power mode [high speed], pass said locked clock signal to said third input/output buffer; a second clock line [CLKO] coupled to the third input/output buffer [514] of the second multiplexor [510] [col. 5, lines 9 - 67, col. 6, lines 1 - 60, fig. 5].

It would have been obvious to one of ordinary skill in art, having the teachings of Challen, and Zhang before him at the time of invention was made, to modify the PLL circuit arrangement for battery saving frequency synthesizer to include a second multiplexor as taught by Zhang in order to obtain dual mode clock alignment and distribution devices bypasses the PLL and generates clock with sufficient margins to accommodate the requirements of the PCI mode and support both both lower speed PCI clocking mode and the higher speed PCI-X clocking mode to provide substantial savings in cost while reducing circuit complexity [co. 3, lines 34 – 51].

38. As to claims 9, 15, and 38, Zhang discloses the step of disabling the phase lock loop, when in first power mode (lower speed or PCI clock mode) which inherently teaches [as per PCI-X specs] including reducing in comparison to a maximum number of bits used available [PCI-X mode] used to represent multimedia data [col. lines 4 – 21].

39. As to claims 10 - 11, 16 - 17, and 39 - 40, Zhang discloses PCI and PCI-X devices therefore he teaches multimedia data including audio, video data [col. 2, lines 56 – 57, col. lines 4 – 21].

40. As to claims 12, and 18, Zhang discloses providing the oscillator signal [CLKin from 502] to the phase locked loop [504], when in the second power mode [high speed or PCI-X], which includes use of maximum number of bits to represent multimedia data [col. 3, lines 33 – 51, fig. 5].

41. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant.

Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

42. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Allowable Subject Matter

43. Claim 50 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

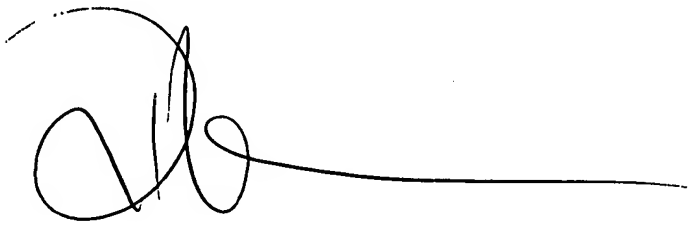
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am - 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
August 24, 2005



A. ELAMIN
PRIMARY EXAMINER